REMARKS

Claims 1-8 were pending in this application as of the Examiner's Office Action to which this Amendment is responsive. Claims 1-8 are rejected.

The below remarks are organized according to the section headings of the Examiner's Detailed Action of Dec. 15, 2006.

1. Claim Rejections – 35 USC § 102

Claims 1 and 6-8 are rejected under 35 USC § 102(b) under the following article (referred to as "Chandra"): A. Chandra et al., "AVPGEN - A Test Generator for Architecture Verification," IEEE Transactions on VLSI Systems, Vol. 3, No. 2, June 1995.

Claims 1 and 6-8 are not anticipated by Chandra for at least the reason that Chandra makes no disclosure or suggestion of bit-slice constraint nodes. The Examiner is referred to section 3.6.1 ("Limited Backward Implication: Bit Slice Operator") of the application, and particularly pages 51-52, where a clear definition of the term bit-slice constraint node is provided. Specifically, the application states (on page 51, lines 19-22):

> A bit-slice operator takes an input variable and selects, for output, the value of a range of bits of the input variable, where the range is specified by two other inputs to the bit-slice operator.

The Examiner is referred to MPEP 2111.01 which states: "the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification" (emphasis added).

The Examiner states that page 190, Figure 4, of Chandra discloses bit-slice constraint nodes. Specifically, the Examiner states (see page 3 of the Examiner's Action):

> [T]he bit-sliced constraint nodes are the nodes of Fig. 4; the first variable is the range of bits that have been bit-sliced; bit-slice is synonymous with parsing that is well known in the industry.

Figure 4 is discussed in section III.A of the Chandra article on page 190. Section III.A states that Figure 4 is created from Figure 3. Chandra describes Figure 3 as follows (see page 190, from last two lines of column 1 to line 11 of column 2):

> Consider the SIGL program in Fig. 3. This program

> specifies one symbolic instruction graph (or graph in short), named ex1, with the following characteristics. The start statement specifies that instruction execution should begin at node n1 of ex1. The graph has two LOAD instructions with labels n1 and n2. The R1 registers of these LOAD instructions are given the names x and y, respectively. The oneof node, n3, specifies that either the ADD or the SUBTRACT be chosen in each test generated from this SIGL program. In either case, the chosen instruction (ADD or SUBTRACT) following the LOADs is constrained to use the registers x and y, that were defined and loaded earlier, for its operands.

As can be seen from the above description, Figure 3 of Chandra describes two LOAD instructions and either an ADD or SUBTRACT instruction. "Load" instructions are well known instructions for loading the contents of a specified memory location into a CPU register. Similarly, "add" and "subtract" are well known instructions for, respectively, adding or substracting two numbers. There is simply no suggestion or teaching in Chandra that the instructions of Figure 3 perform a bit-slice operation as defined by the applicant.

The Examiner states that "the first variable is the range of bits that have been bit-sliced." See above quotation from the Examiner's Action. Applicant is unclear as to which variable is "first." However, applicant will assume that the Examiner is referring to the leftmost variable in each node of Figure 4. For the top node of Figure 4 (a node that performs a "LOAD"), the leftmost variable is "x;" for the middle node of Figure 4 (a node that performs a "LOAD"), the leftmost variable is "y;" and for the bottom node of Figure 4 (the node that performs a "oneof" ADD or SUBTRACT), the leftmost variable is "R1." Applicant directs the Examiner's attention to the fact that Chandra, as shown in the above quotation, refers to "x" and "y" as "names" for the "R1 registers of these LOAD instructions." Thus, the names "x," "y" and "R1" are used to refer to registers that are the operands of the LOAD, ADD and SUBTRACT operations. There is simply no suggestion or teaching in Chandra that these names specify a range of bits who values are to be extracted through a bit-slice operation.

The Examiner makes the unsubstantiated statement that "bit-slice is synonymous with parsing that is well known in the industry." See above quotation from the Examiner's Action. Parsing is described, in Chandra, as the process by which the input language of Figure 3 (written in SIGL) is transformed into the graph of Figure 4. Specifically, Chandra states:

> The SIGL program is read into the AVPGEN system by the parser (see Fig. 2). A symbolic instruction graph structure is created as depicted in Fig. 4.

Applicants respectfully direct the Examiner's attention to MPEP 2144.03 ("Reliance on Common Knowledge in the Art or 'Well Known' Prior Art") which states:

> Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known.

Rather than being "unquestionable," the statement, that a performing a bit-slice operation is synonymous with parsing, is clearly incorrect. How can performance of a bit-slice operation be the same as transforming SIGL into a graph structure?

Where the facts sought to be introduced are not unquestionable, MPEP 2144.03 states the following:

> It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art.

If the Examiner wishes to continue to use the above-quoted unsubstantiated statement, applicants respectfully request the Examiner cite prior art references to support it.

Because claims 1 and 6-8 are allowable, claims 2-5, that are dependent upon claim 1 and therefore only add additional limitations, are also allowable for at least the same reasons.

2. Summary

Applicants respectfully submit that all objections and rejections have been traversed and request a Notice of Allowance.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 502584 referencing docket number 06816.0506CON2.

Respectfully submitted,

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